ABSTRACT

The serial scaleable bandwidth interconnect (SBI336S) bus provides a 777.6 MHz point-to-point LVDS serial interface that supports a variety of traffic types including support for Fractional links. 8B/10B coding is used on the serial link to provide codes to transmit additional control information across the serial interface. The SBI336S bus encodes ADD BUS clock master timing from the PHY device to the Link Layer device over the DROP BUS. The SBI336S bus can also provide an in-band communication channel between devices.